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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/693,093	10/23/2003	Jy-Der David Tai	13998 B	8452

7590 05/22/2006

CHARLES E. BAXLEY, ESQUIRE
Third Floor
90 John Street
New York, NY 10038

EXAMINER	
THOMAS, LUCY M	

ART UNIT	PAPER NUMBER
2836	

DATE MAILED: 05/22/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/693,093	TAI, JY-DER DAVID	
	Examiner	Art Unit	
	Lucy Thomas	2836	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 February 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3 and 5-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3 and 5-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, 3, and 5-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Poe et al. (US 6,646,847) in view of Baylac et al. (US 5,187,631) and Sasahara et al. (US 5,856,756). Regarding Claim 1, Poe et al. discloses a short circuit detecting and protecting circuit (Figures 1-3) comprising a switching unit 112, G1 for obtaining input signals, a comparator 104, U1 including a first input terminal coupled to said switching unit, an output terminal and a second input terminal, and including an internal voltage, a load (R_LOAD) connected to said first input terminal of said comparator, means for detecting a voltage difference (see R_SENSE in Figure 2 and 3) between said first and said second input terminal of the comparator, said detecting means includes a detecting resistor R_SENSE coupled between said first and said second input terminals of said comparator, to generate and provide two voltage signals to said first and said second input terminals of said comparator respectively, said comparator comparing the voltage difference between said first and said second terminal of said comparator and internal voltage of said comparator, to detect short circuit or overload situation (Column2, lines 24-34, 47-67, Column 3, lines 1-37).

Poe et al does not disclose a control transistor coupled between said switching unit and said second input terminal of said comparator, and the switching unit including a first transistor coupled to said first input terminal of said comparator to obtain one of the input signals, and a second transistor coupled to said control transistor to obtain the other input signal.

Baylac discloses a short circuit detecting and protecting circuit (see Figure 2) comprising a switching unit 1, a comparator 6, a load 2 coupled to an input terminal of the comparator, and a control transistor 7 coupled between the switching unit and the input terminal of the comparator. It would have been obvious to one of ordinary skill in the art to include a transistor coupled between the switching unit and the second input terminal of the comparator to control the timing of the input signals, because it is known in the art to add an active device such as a transistor to a reference circuit to increase flexibility of the response over current events.

Sasahara discloses a switching unit including a first transistor N1 coupled to a first input terminal of a comparator to obtain one of the input signals, and a second transistor p5 coupled to a control transistor p4 to obtain the other input signal (Figure 1). It would have been obvious to those skilled in the art at the time the invention was made to provide the switching unit of Sasahara in the circuit of Poe to increase the range of voltages to which the comparator can respond. The Baylac reference discloses a control transistor 7 coupled between the switching unit and the input terminal of the comparator, and both Poe and Baylac discloses a load. Therefore the references, Poe, Baylac, and Sasahara, in combination, meet the claim limitations of the amended claim.

Regarding Claim 3, Sasahara et al. discloses a switching unit, which is a CMOS, having a pMOS p1 and an nMOS N1 (Figure 1).

Regarding Claim 5, Poe et al. discloses a short circuit detecting and protecting circuit further comprising a divider resistor R3 coupled between the switching unit and said second input terminal of said comparator, to divide the signals.

Regarding Claim 6, Poe et al. discloses a short circuit detecting and protecting circuit, wherein the load resistor R_LOAD coupled to the first input terminal of the comparator and ground.

3. Claims 7 -11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gonthier et al. (US 2004/0066594 A1) in view of Baylac et al. (US 5,187,631). Regarding Claim 7, Gonthier discloses a short circuit detecting and protecting circuit (Figure 3) comprising a switching unit including a first and second switching transistors T1, T2 for obtaining a first and a second input signals respectively, a first and a second comparators 37, 39 each including a first and a second input terminals 40, 38, 36, 43 and an output terminal, the first input terminal of the first comparator 37 being coupled to a control diode 32 via a first resistor 41, the second input terminal of the comparator 39 being coupled to a second control diode 33 via a second resistor 44, a load 21 coupled between the second input terminal of the first comparator and the first input terminal of the second comparator, and a first detecting resistor 45 coupled between said first input terminal 40 of said first comparator 37 and said second input terminal 43 of said second comparator 39, to actuate either said first or said second comparator to output control signals.

Gonthier does not disclose a second detecting resistor in Figure 3, but discloses an alternative with voltage dividers to each input terminal 40 and 43 respectively (0053, lines 7-13), and the voltage divider provides the second detecting resistor. Gonthier fails to disclose a first and second control transistors. Baylac teaches a short circuit detecting and protecting circuit (see Figure 2) comprising a switching unit 1, a comparator 6, a load 2, and a control transistor 7. It would have been obvious to those skilled in the art at the time the invention was made to provide a first and a second control transistors coupled to said first and said second transistors of said switching unit respectively to control the timing of the input signals to increase flexibility of the response over current events. Gonthier reference discloses a load coupled between the second input terminal of the first comparator and the first input terminal of the second comparator as recited in the amended claim and Baylac reference teaches the use of control transistor coupled between the comparator and the switching unit. Therefore, Gonthier and Baylac references, in combination, meet the limitations of the amended claim.

Regarding Claim 8, Gonthier discloses a short circuit detecting and protecting circuit, wherein said first switching transistor is a MOS, and a second switching transistor is a MOS, both of same conduction type, pMOS or nMOS (0048, lines 1-3). It would have been obvious to those skilled in the art at the time the invention was made to provide both a pMOS and nMOS transistor and configure the circuit accordingly based on the polarity of the supply voltage to each transistor in the circuit. Furthermore, it is known to mix polarity in push-pull buffer circuits.

Regarding Claim 9, Gonthier discloses a short circuit detecting and protecting circuit further comprising an over current control means for switching off said short circuit detecting and protecting circuit when receiving said output control signals from either said first 37 or said second comparator 39 (0057, lines 20-24).

Regarding Claim 10, Gonthier discloses a short circuit detecting and protecting circuit, wherein said over current control means includes an OR gate 42 coupled between said first and said second comparators 37, 39 (0052, lines 1-4).

Regarding Claim 11, Gonthier discloses a short circuit detecting and protecting circuit, wherein said over current control means further includes a first and second control circuits 26 (also see Figure 1B for details of 26) coupled to said first and said second switching transistors T1, T2 of said switching unit respectively and coupled to said OR gate.

Response to Arguments

4. Applicant's arguments filed on 2/27/2006 have been fully considered.

The Applicant states that the cited art fail to teach a control transistor. However, to meet the limitation, a control transistor, which detects the time where the input signals flow to the comparator, the Baylac reference was introduces to teach a control transistor coupled between the switching unit and the comparator, which would necessarily detect the flowing of the input signals to the comparator.

Regarding Applicant statement that the Gonthier reference fails to teach a second detecting resistor: In Figure 3, Gonthier does not explicitly disclose a second detecting resistor, however, an alternative with voltage dividers to each input terminal of

the comparator, respectively (0053, lines 7-13), and the voltage divider provides the second detecting resistor.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lucy Thomas whose telephone number is 571-272-6002. The examiner can normally be reached on Monday - Friday 8:00 AM - 4:30 PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Brian Sircus can be reached on 571-272-2058. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

LT
May 12, 2006

PHUONG T. VU
PRIMARY EXAMINER